2.9 inch
E-paper Display Series

GooDisplay®

GDEY029F51H

Dalian Good Display Co., Ltd.

Product Specifications

Customer	**Standard**
Description	**2.9" EPAPER DISPLAY**
Model Name	**GDEY029F51H**
Date	**2023 / 03 / 21**
Revision	**1.0**

	Design Engineering		
	Approval	**Check**	**Design**
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1. Over View

GDEY029F51H is a reflective electrophoretic technology display module on an active matrix TFT substrate. The panel is capable of displaying black, white, yellow and red images depending on the associated lookup table used. The circuitry on the panel includes an integrated gate and source driver, timing controller, oscillator, DC-DC boost circuit, and memory to store the frame buffer and lookup tables, and additional circuitry to control VCOM and BORDER settings.

2. Features

- Highlight Red and Yellow color
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Antiglare hard-coated front-surface
- Low current deep sleep mode
- On chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I^2C signal master interface to read external temperature sensor
- Available in COG package

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.9	Inch	
Display Resolution	168(H)×384 (V)	Pixel	Dpi:144
Active Area	29.57×6 7.58	mm	
Pixel Pitch	0.176×0.176	mm	
Pixel Configuration	Rectangle		
Outline Dimension	35.57(H)×79.98(V) ×1.0(D)	mm	
Weight	5.29±0.5	g	

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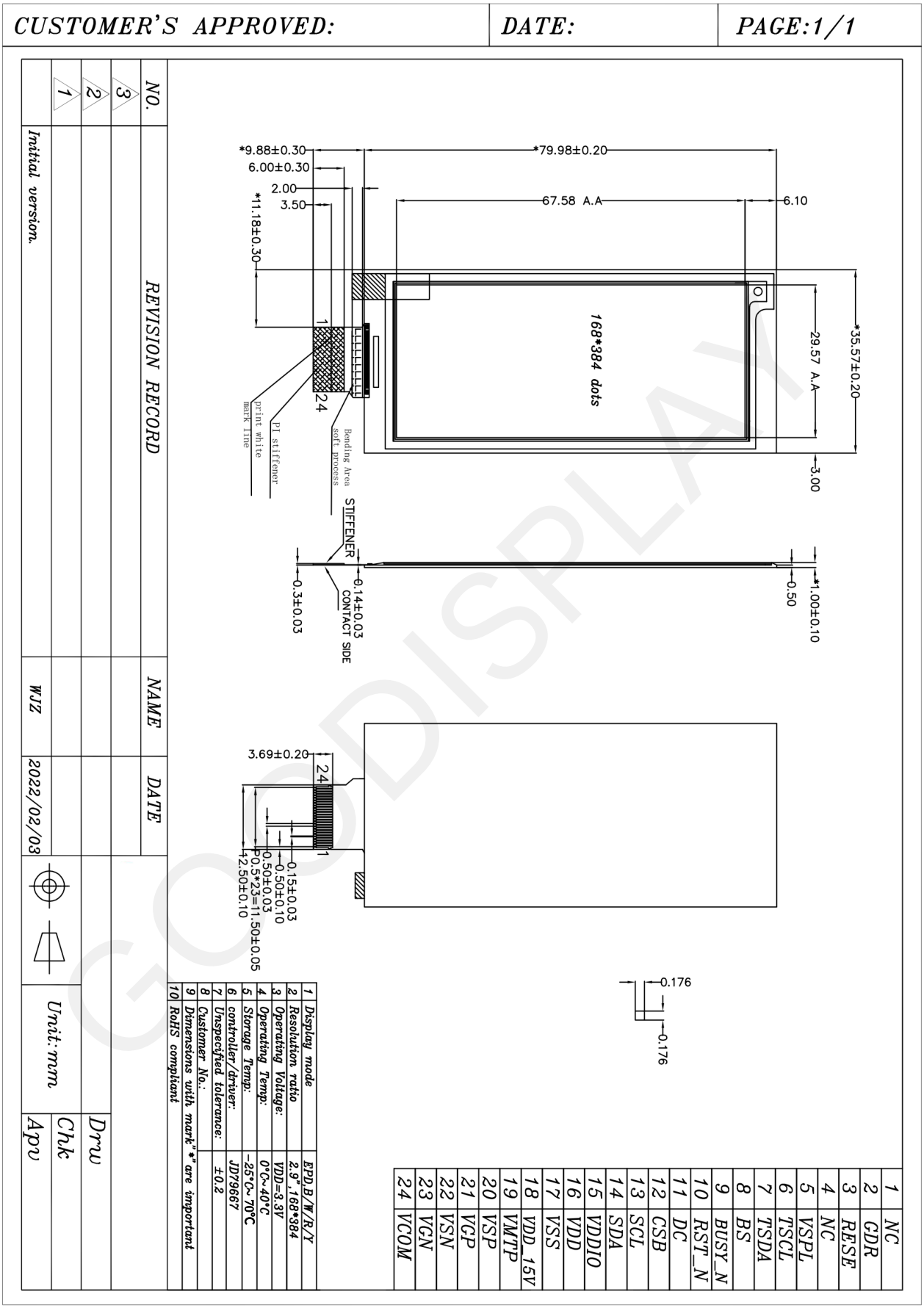
4. Mechanical Drawing of EPD module



5. Input /Output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	This pin is N-MOS gate control.	
3	RESE	P	Current sense input for control loop.	
4	NC	NC	Do not connect with other NC pins	Keep Open
5	VSPL	P	Positive source voltage	
6	TSCL	O	I^2C clock for external temperature sensor (I^2C interface need external pull high resistance.) Must pull high or low if not used.	
7	TSDA	I/O	I^2C data for external temperature sensor (I^2C interface need external pull high resistance.) Must pull high or low if not used.(Default low)	
8	BS	I	Input interface setting.	
9	BUSY_N	O	This pin indicates the driver status.	
10	RST_N	I	Global reset pin. Low reset. (normal pull high)	
11	DC	I	Serial communication Command/Data input	
12	CSB	I	Serial communication chip select.	
13	SCL	I	Serial communication clock input.	
14	SDA	I/O	Serial communication data input.	
15	VDDIO	P	IO voltage supply	
16	VDD	P	Digital/Analog power.	
17	VSS	P	Ground	
18	VDD_15V	P	1.5V voltage input &output	
19	VMTP	P	MTP program power (10.1V)	
20	VSP	P	Positive source voltage	
21	VGP	P	Positive gate voltage	
22	VSN	P	Negative Source driving voltage	
23	VGN	P	Negative gate voltage	
24	VCOM	O	VCOM driving voltage	

Note: I: Input, O: Output, P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output,I/O: Input / Output. PS: Power Setting, C: Capacitor pin.

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6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VDD, AVDD,VDDIO, VDD1,VPP	-0.3 to +6.0	V
Logic Input voltage	VI	-0.3 to VDDIO+0.3	V
Operating Temp range	TOPR	0 to +40	ºC
Storage Temp range	TSTG	-25 to +70	ºC
Optimal Storage Humidity	HSTGo	55±10	%RH

Note: Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied. Exposing device to the absolute maximum ratings in a long period of time may degrade the device and affect its reliability.

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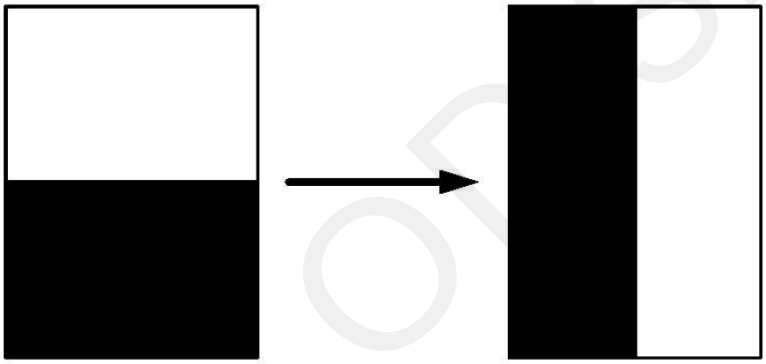
6.2 Panel DC Characteristics

Parameter	Symbol	Conditions	Applicable pin	Min.	Typ.	Max	Units
Single ground	V_{SS}	-		-	0	-	V
Logic supply voltage	V_{IO}	-	VIO	2.3	3.3	3.6	V
Core logic voltage	V_{DD}		VDD	2.3	3.3	3.6	V
High level input voltage	V_{IH}	-	-	$0.7V_{IO}$	-	V_{IO}	V
Low level input voltage	V_{IL}	-	-	GND	-	$0.3V_{DD}$	V
High level output voltage	V_{OH}	IOH = 400uA	-	V_{IO} -0.4	-	-	V
Low level output voltage	V_{OL}	IOL = -400uA	-	GND	-	GND +0.4	V
Typical power	P_{TYP}	V_{CI} =3.3V	-	-	9.9	-	mW
Deep sleep mode	P_{STPY}	V_{CI} =3.3V	-	-	0.003	-	mW
Typical operating current	Iopr_V_{CI}	V_{CI} =3.3V	-	-	3.0	-	mA
Image update time	-	25 ℃	-	-	20	-	sec
Stand-by current	Ist_V_{DD}		-	-	1	5	uA

Notes: 1. The typical power is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern.



2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Good Display.

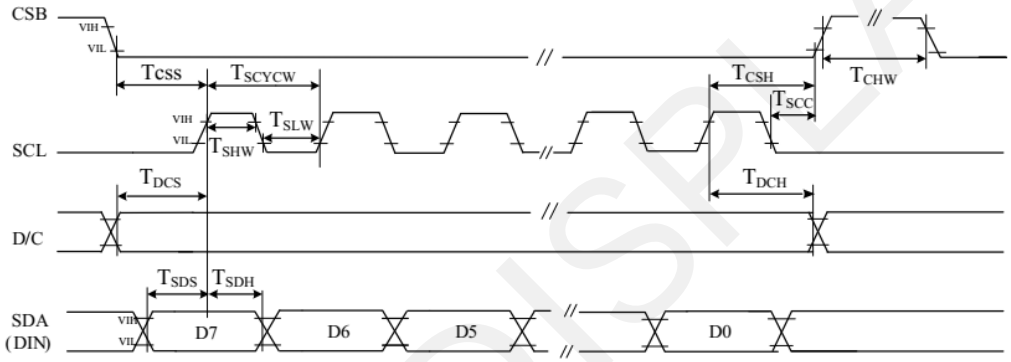
6.3 AC Characteristics

6.3.1 MCU Interface Selection

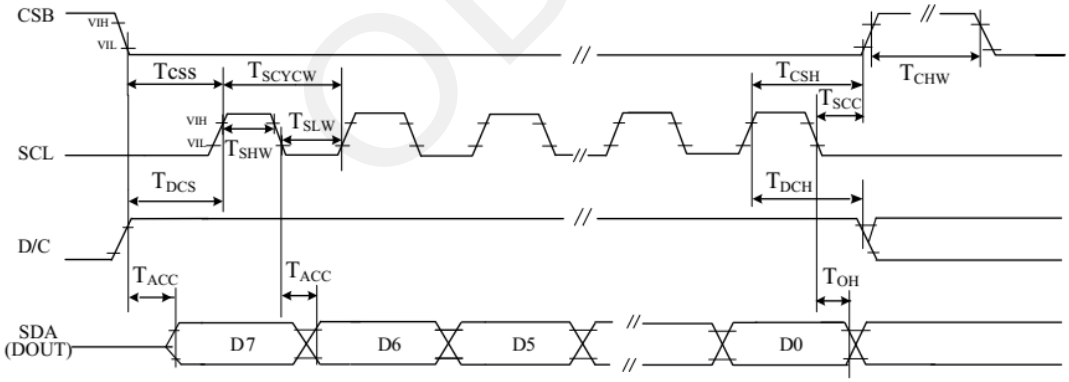
The 3-wire/4-wire serial port as communication interface for all the function and command setting. 3-wire/4-wire engine act as a "slave mode" for all the time, and will not issue any command to the 3-wire/4-wire bus itself.

Under read mode, 3-wire/4-wire engine will return the data during "Data phase". The returned data should be latched at the rising edge of SCL by external controller. Data in the "Hi-Z phase" will be ignored by 3-wire/4-wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under "Hi-Z phase" and "Data phase".

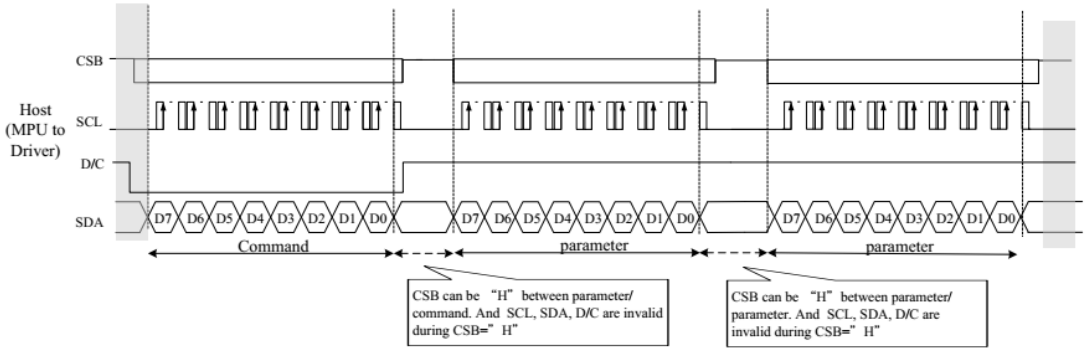
6.3.2 MCU Serial Interface (4-wire SPI)



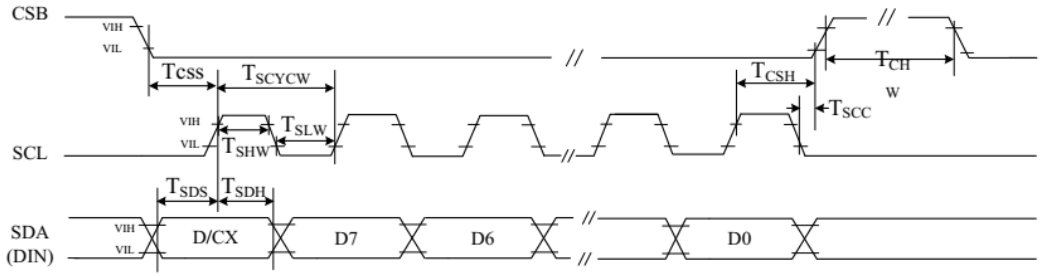
4 pin serial interface characteristics(write mode)



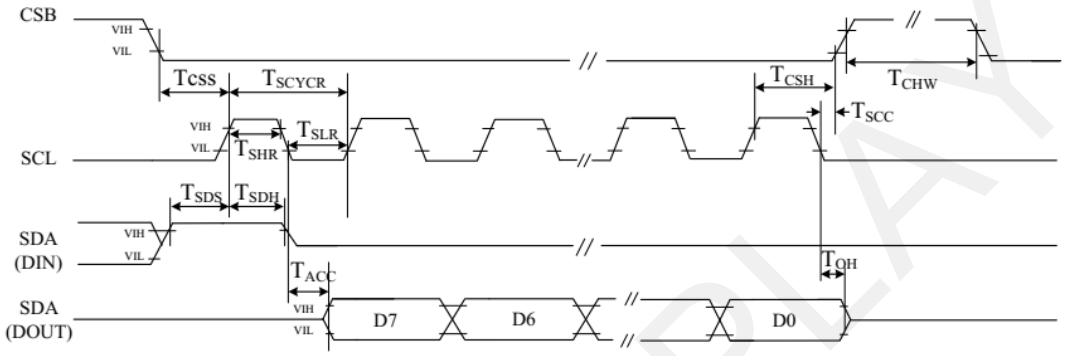
4 pin serial interface characteristics(read mode)



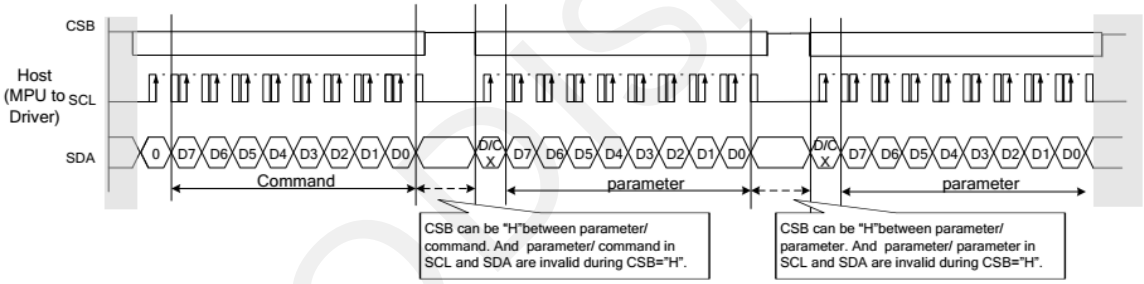
6.3.3 MCU Serial Interface (3-wire SPI)



3 pin serial interface characteristics (write mode)



3 pin serial interface characteristics (read mode)



7. Command Table

Address	command						Bit					
		R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
R00H	Panel setting (PSR)	W	0	0	0	0	0	0	0	0	0	00H
		W	1	RES[1]	RES[0]	PST_MODE	-	UD	SHL	SHD_N	RST_N	0Fh
		W	1	LUT_EN	-	FOPT	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	09h
R01H	Power setting (PWR)	W	0	0	0	0	0	0	0	0	1	01H
		W	1	-	-	-	-	V_MODE	VSC_EN	VDS_EN	VDG_EN	07h
		W	1	-	-	-	-	-	-	VGPN [1]	VGPN [0]	00h
		W	1	-	VSPL_0[6]	VSPL_0[5]	VSPL_0[4]	VSPL_0[3]	VSPL_0[2]	VSPL_0[1]	VSPL_0[0]	00h
		W	1	-	VSP_1[6]	VSP_1 [5]	VSP_1 [4]	VSP_1 [3]	VSP_1 [2]	VSP_1 [1]	VSP_1 [0]	00h
		W	1	-	VSN_1[6]	VSN_1[5]	VSN_1[4]	VSN_1[3]	VSN_1[2]	VSN_1[1]	VSN_1[0]	00h
		W	1	-	VSPL_1[6]	VSPL_1[5]	VSPL_1[4]	VSPL_1[3]	VSPL_1[2]	VSPL_1[1]	VSPL_1[0]	00h
R02H	Power OFF(POF)	W	0	0	0	0	0	0	0	1	0	02H
		W	1	-	-	-	-	-	-	-	EDSE	00h
R03H	Power off Sequence Setting(PFS)	W	0	0	0	0	0	0	0	1	1	03H
		W	1	T_VDS_OFF2[1:0]		T_VDPG_OFF[1:0]		T_VDS_ON[1:0]		T_VDS_OFF[1:0]		00h
		W	1	VGP_LEN[3:0]				VGP_EXT[3:0]				54
		W	1	XON_DLY				XON_LEN				44
R04H	Power ON (PON)	W	0	0	0	0	0	0	1	0	0	04H
R06H	Booster Soft Start (BTST)	W	0	0	0	0	0	0	1	1	0	06H
		W	1	-	-	-	-	PHB_SFT[1:0]		PHA_SFT[1:0]		00h
		W	1	-	-	PHA_ON[5:0]						02h
		W	1	-	-	PHA_OFF[5:0]						07h
		W	1	-	-	PHB_ON[5:0]						02h
		W	1	-	-	PHB_OFF[5:0]						07h
		W	1	-	-	PHC_ON[5:0]						02h
		W	1	-	-	PHC_OFF[5:0]						07h
R07H	Deep Sleep(DSLP)	W	0	0	0	0	0	0	1	1	1	07H
		W	1	1	0	1	0	0	1	0	1	A5h
R10H	Data Start transmission (DTM)	W	0	0	0	0	1	0	0	0	0	10H
		W	1	#	#	#	#	#	#	#	#	00H
R11H	Data Stop (DSP)	W	0	0	0	0	1	0	0	0	1	11H
		R	1	Data_flag	-	-	-	-	-	-	-	--
R12H	Display Refresh (DRF)	W	0	0	0	0	1	0	0	1	0	12H
		W	1	-	-	-	-	-	Gate_seq	-	AC/DC VCOM	00H
R17H	Auto sequence (AUTO)	W	0	0	0	0	1	0	1	1	1	17H
		W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	A5h
R30H	PLL control (PLL)	W	0	0	0	1	1	0	0	0	0	30H
		W	1	-	-	-	-	Dyna		FR[2:0]		02h
R40H	Temperature Sensor Command (TSC)	W	0	0	1	0	0	0	0	0	0	40H
		R	1	D10/TS[7]	D9/TS[7]	D8/TS[6]	D7/TS[5]	D6/TS[4]	D5/TS[3]	D4/TS[2]	D3/TS[1]	--
		R	1	D2/ TS[9]	D1/TS[8]	D0	-	-	-	-	-	--
R41H	Temperature Sensor Calibration (TSE)	W	0	0	1	0	0	0	0	0	1	41H
		W	1	TSE	-	-	TO[4]	TO[3]	TO[2]	TO[1]	TO0]	00h
R42H	Temperature Sensor Write (TSW)	W	0	0	1	0	0	0	0	1	0	42H
		W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
		W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
		W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h
R43H	Temperature Sensor	W	0	0	1	0	0	0	0	1	1	43H

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	Read (TSR)	R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	--
		R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	--
R50H	VCOM and DATA interval setting (CDI)	W	0	0	1	0	1	0	0	0	0	50H
		W	1	VBD[2]	VBD[1]	VBD[0]	DDX	CDI[3]	CDI[2]	CDI[1]	CDI[0]	97h
R51H	Lower Power Detection (LPD)	W	0	0	1	0	1	0	0	0	1	51H
		R	1	-	-	-	-	-	-	-	LPD	--
R61H	Resolution setting(TRES)	W	0	0	1	1	0	0	0	0	1	61H
		W	1	-	-	-	-	-	-	HRES(9)	HRES(8)	00h
		W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	HRES(2)	0	0	00h
		W	1	-	-	-	-	-	-	VRES(8)	VRES(0)	00h
		W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00h
R65H	Gate/Source Start Setting(GSST)	W	0	0	1	1	0	0	1	0	1	65H
		W	1	-	-	-	-	-	-	S_start(9)	S_start(8)	00h
		W	1	S_start(7)	S_start(6)	S_start(5)	S_start(4)	S_start(3)	S_start(2)	0	0	00h
		W	1	-	-	-	-	-	-	G_start(9)	G_start(8)	00h
		W	1	G_start(7)	G_start(6)	G_start(5)	G_start(4)	G_start(3)	G_start(2)	G_start(1)	G_start(0)	00h
R70H	REVISION (REV)	W	0	0	1	1	1	0	0	0	0	70H
		R	1	0	0	0	0	0	0	1	1	05h
		R	1	0	0	0	0	0	0	1	0	02h
		R	1	0	0	0	0	0	0	0	1	01h
R80H	Auto Measure Vcom (AMV)	W	0	1	0	0	0	0	0	0	0	80 H
		W	1	P[1]	P[0]	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	00h
R81H	Vcom Value (VV)	W	0	1	0	0	0	0	0	0	1	81H
		R	1	-	VV[6]	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	--
R82H	Vcom_DC Setting register(VDCS)	W	0	1	0	0	0	0	0	1	0	82H
		W	1	MTP_VCM	VDCS[6]	VDCS[5]	VDCS[4]	VDCS[3]	VDCS[2]	VDCS[1]	VDCS[0]	00h
R83H	Partial Window (PTLW)	W	0	1	0	0	0	0	0	1	1	83H
		W	1	-	-	-	-	-	-	HRST(9)	HRST(8)	00h
		W	1	HRST(7)	HRST(6)	HRST(5)	HRST(4)	HRST(3)	HRST(2)	0	0	00h
		W	1	-	-	-	-	-	-	HRED(9)	HRED(8)	00h
		W	1	HRED(7)	HRED(6)	HRED(5)	HRED(4)	HRED(3)	HRED(2)	0	0	00h
		W	1	-	-	-	-	-	-	VRST(9)	VRST(8)	00h
		W	1	VRST(7)	VRST(6)	VRST(5)	VRST(4)	VRST(3)	VRST(2)	VRST(1)	VRST(0)	00h
		W	1	-	-	-	-	-	-	VRST(9)	VRST(8)	00h
		W	1	VRST(7)	VRST(6)	VRST(5)	VRST(4)	VRST(3)	VRST(2)	VRST(1)	VRST(0)	00h
		W	1	-	-	-	-	-	-	-	PMOD	00h
R90H	Program mode(PGM)	W	0	1	0	0	1	0	0	0	0	90H
R91H	Active Program(APG)	W	0	1	0	0	1	0	0	0	1	91H
R92H	Read MTP data (RMTP)	W	0	1	0	0	1	0	0	1	0	92H
		R	1	#	#	#	#	#	#	#	#	-
R9EH	REVISION2 (REV2)	W	0	1	0	0	1	1	1	1	0	9EH
		R	1	0	0	0	0	0	0	0	1	01h
R9FH	Read MTP Reserved Bytes(RMRB)	W	0	1	0	0	1	1	1	1	1	9FH
		R	1	#	#	#	#	#	#	#	#	-
RE3H	Power saving(PWS)	W	0	1	1	1	0	0	0	1	1	E3H
		W	1	VCOM_W [3]	VCOM_W [2]	VCOM_W [1]	VCOM_W [0]	SD_W[3]	SD_W[2]	SD_W[2]	SD_W[0]	00h
RE4H	LVD voltage Select(LVSEL)	W	0	1	1	1	0	0	1	0	0	E4H
		W	1	-	-	-	-	-	-	LVD_SEL [1]	LVD_SEL [0]	03h
		R	1	Chk_CRC[7:0]								00h
		R	1	MTP_CRC[7:0]								00h

R00H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PSR	W	0	0	0	0	0	0	0	0	0	00H
1st Parameter	W	1	RES[1]	RES[0]	PST_MODE	-	UD	SHL	SHD_N	RST_N	0Fh
2nd Parameter	W	1	LUT_EN	-	FOPT	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	09h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

1st parameter

Bit	Name	Description
0	RST_N	RST_N function 1: no effect. (default) 0: Booster OFF, Register data are set to their default values, and Source/Boder/Vcom: floating
1	SHD_N	SHD_N function 0 : Booster OFF, register data are kept, and Source/Boder/Vcom are kept 0V or floating. 1 : Booster on. (default)
2	SHL	SHL function 0: Shift left; First data=Sn→Sn-1 →…→S2→Last data=S1. 1: Shift right: First data=S1→S2 →…→Sn-1→Last data=Sn. (default)
3	UD	UD function 0:Scan down; First line=Gn→Gn-1 →…→G2→Last line=G1. 1:Scan up; First line=G1→G2 →…→Gn-1→Last line=Gn. (default)
5	PST_MODE	Power switch operation mode 0:Power switching time in the period of frame scanning.(default) 1:Power switching time in the external period before frame scanning.
7-6	RES[1,0]	Resolution setting 00: Display resolution is 200x384 (default) 01: Display resolution is 184x384 10: Display resolution is 168x384 11: Display resolution is 200x200

2nd parameter

Bit	Name	Description
0	VC_LUTZ	VCOM status function 0 : No effect 1 : After refreshing display,the output of VCOM is set to floating automatically (default)
1	NORG	VCOM status function 0 : No effect (default) 1 : After refreshing display, VCOM is tied to GND before power off
2	TIEG	VGN power off status function 0 : No effect (default) 1 : Power off, VGN will be tied to GND
3	TS_AUTO	Temperature sensing will be activated automatically one time 0 : Before enabling booster,Temperature Sensor will be activated automatically one time. 1 : When RST_N low to high,Temperature Sensor will be activated automatically one time. (default)
4	VCMZ	VCOM status function 0 : No effect (default) 1 : VCOM is always floating
5	FOPT	FOPT function 0: Scan 1 frame after waveform finished(default) 1: No scan after waveform finished and switch the source channel output to Hiz.

Priority of VCOM setting: VCMZ > NORG > FOPT > VC_LUTZ

FOPT setting is part of refreshing display.
FOPT: Power off floating.

Notes:
1. Non-select gate line keep at VGN for DSP/DRF and AMV
2. Dummy source line follow LUTC for DSP/DRF
3. When SHD_N become low, DCDC will turn off. Register and SRAM data will keep until VDD turn off.SD output and VCOM will base on previous condition. It may have two condition:0V or floating.
4. When RST_N become low, driver will reset. All register will reset to default value. All of the driver's functions will disable. Source/Gate/Border/VCOM will be released to floating

Restriction

R01H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWR	W	0	0	0	0	0	0	0	0	1	01h
1st Parameter	W	1	-	-	-	-	V_MODE	VSC_EN	VDS_EN	VDG_EN	07h
2nd Parameter	W	1	-	-	-	-	-	-	VGPN [1]	VGPN [0]	00h
3rd Parameter	W	1	-	VSPL_0 [6:0]							00h
4th Parameter	W	1	-	VSP_1 [6:0]							00h
5th Parameter	W	1	-	VSN_1 [6:0]							00h
6th Parameter	W	1	-	VSPL_1 [6:0]							00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

1st Parameter:

Bit	Name	Description
0	VDG_EN	Gate power selection. 0 : External gate power from VGP/VGN pins. 1 : Internal DCDC function for generate VGP/VGN. (default)
1	VDS_EN	Source power selection. 0 : External source power from VSP/VSN pins. 1 : Internal regulator function for generate VSP/VSN (default)
2	VSC_EN	Source LV power selection. 0 : External source power from VSPL pins. 1 : Internal regulator function for generate VSPL (default)
3	V_MODE	Source Power switching mode. 0: Mode0(default) 1: Mode1

2nd Parameter:

Bit	Name	Description
1-0	VGPN	VGPN Voltage Level. 00: VGP=20 v, VGN=-20v (default) 01: VGP=17 v, VGN=-17v 10: VGP=15 v, VGN=-15v 11: VGP=10 v, VGN=-10v

3rd & 4th & 6th Parameter: Internal VSP_1/VSPL_0/ VSPL_1 power selection

Bit	Name	Description
6-0	VSP_1 & VSPL_0 & VSPL_1	**Internal VSP & VSPL power selection.**

bit[6:0]		Voltage(V)	bit [6:0]		Voltage(V)	bit [6:0]		Voltage(V)
0000000	00h	3	0101001	29h	7.1	1010010	52h	11.2
0000001	01h	3.1	0101010	2Ah	7.2	1010011	53h	11.3
0000010	02h	3.2	0101011	2Bh	7.3	1010100	54h	11.4
0000011	03h	3.3	0101100	2Ch	7.4	1010101	55h	11.5
0000100	04h	3.4	0101101	2Dh	7.5	1010110	56h	11.6
0000101	05h	3.5	0101110	2Eh	7.6	1010111	57h	11.7
0000110	06h	3.6	0101111	2Fh	7.7	1011000	58h	11.8
0000111	07h	3.7	0110000	30h	7.8	1011001	59h	11.9
0001000	08h	3.8	0110001	31h	7.9	1011010	5Ah	12
0001001	09h	3.9	0110010	32h	8	1011011	5Bh	12.1
0001010	0Ah	4	0110011	33h	8.1	1011100	5Ch	12.2
0001011	0Bh	4.1	0110100	34h	8.2	1011101	5Dh	12.3
0001100	0Ch	4.2	0110101	35h	8.3	1011110	5Eh	12.4
0001101	0Dh	4.3	0110110	36h	8.4	1011111	5Fh	12.5
0001110	0Eh	4.4	0110111	37h	8.5	1100000	60h	12.6
0001111	0Fh	4.5	0111000	38h	8.6	1100001	61h	12.7
0010000	10h	4.6	0111001	39h	8.7	1100010	62h	12.8
0010001	11h	4.7	0111010	3Ah	8.8	1100011	63h	12.9
0010010	12h	4.8	0111011	3Bh	8.9	1100100	64h	13
0010011	13h	4.9	0111100	3Ch	9	1100101	65h	13.1
0010100	14h	5	0111101	3Dh	9.1	1100110	66h	13.2
0010101	15h	5.1	0111110	3Eh	9.2	1100111	67h	13.3

0010110	16h	5.2	0111111	3Fh	9.3	1101000	68h	13.4
0010111	17h	5.3	1000000	40h	9.4	1101001	69h	13.5
0011000	18h	5.4	1000001	41h	9.5	1101010	6Ah	13.6
0011001	19h	5.5	1000010	42h	9.6	1101011	6Bh	13.7
0011010	1Ah	5.6	1000011	43h	9.7	1101100	6Ch	13.8
0011011	1Bh	5.7	1000100	44h	9.8	1101101	6Dh	13.9
0011100	1Ch	5.8	1000101	45h	9.9	1101110	6Eh	14
0011101	1Dh	5.9	1000110	46h	10	1101111	6Fh	14.1
0011110	1Eh	6	1000111	47h	10.1	1110000	70h	14.2
0011111	1Fh	6.1	1001000	48h	10.2	1110001	71h	14.3
0100000	20h	6.2	1001001	49h	10.3	1110010	72h	14.4
0100001	21h	6.3	1001010	4Ah	10.4	1110011	73h	14.5
0100010	22h	6.4	1001011	4Bh	10.5	1110100	74h	14.6
0100011	23h	6.5	1001100	4Ch	10.6	1110101	75h	14.7
0100100	24h	6.6	1001101	4Dh	10.7	1110110	76h	14.8
0100101	25h	6.7	1001110	4Eh	10.8	1110111	77h	14.9
0100110	26h	6.8	1001111	4Fh	10.9	1111000	78h	15
0100111	27h	6.9	1010000	50h	11	other		15
0101000	28h	7	1010001	51h	11.1			

5th Parameter: Internal VSN_1 power selection

Bit	Name	Description
6-0	VSN_1	**Internal VSN power selection.**

bit[6:0]		Voltage(V)	bit [6:0]		Voltage(V)	bit [6:0]		Voltage(V)
0000000	00h	-3	0101001	29h	-7.1	1010010	52h	-11.2
0000001	01h	-3.1	0101010	2Ah	-7.2	1010011	53h	-11.3
0000010	02h	-3.2	0101011	2Bh	-7.3	1010100	54h	-11.4
0000011	03h	-3.3	0101100	2Ch	-7.4	1010101	55h	-11.5
0000100	04h	-3.4	0101101	2Dh	-7.5	1010110	56h	-11.6
0000101	05h	-3.5	0101110	2Eh	-7.6	1010111	57h	-11.7
0000110	06h	-3.6	0101111	2Fh	-7.7	1011000	58h	-11.8
0000111	07h	-3.7	0110000	30h	-7.8	1011001	59h	-11.9
0001000	08h	-3.8	0110001	31h	-7.9	1011010	5Ah	-12
0001001	09h	-3.9	0110010	32h	-8	1011011	5Bh	-12.1
0001010	0Ah	-4	0110011	33h	-8.1	1011100	5Ch	-12.2
0001011	0Bh	-4.1	0110100	34h	-8.2	1011101	5Dh	-12.3
0001100	0Ch	-4.2	0110101	35h	-8.3	1011110	5Eh	-12.4
0001101	0Dh	-4.3	0110110	36h	-8.4	1011111	5Fh	-12.5
0001110	0Eh	-4.4	0110111	37h	-8.5	1100000	60h	-12.6
0001111	0Fh	-4.5	0111000	38h	-8.6	1100001	61h	-12.7
0010000	10h	-4.6	0111001	39h	-8.7	1100010	62h	-12.8
0010001	11h	-4.7	0111010	3Ah	-8.8	1100011	63h	-12.9
0010010	12h	-4.8	0111011	3Bh	-8.9	1100100	64h	-13
0010011	13h	-4.9	0111100	3Ch	-9	1100101	65h	-13.1
0010100	14h	-5	0111101	3Dh	-9.1	1100110	66h	-13.2
0010101	15h	-5.1	0111110	3Eh	-9.2	1100111	67h	-13.3
0010110	16h	-5.2	0111111	3Fh	-9.3	1101000	68h	-13.4
0010111	17h	-5.3	1000000	40h	-9.4	1101001	69h	-13.5
0011000	18h	-5.4	1000001	41h	-9.5	1101010	6Ah	-13.6
0011001	19h	-5.5	1000010	42h	-9.6	1101011	6Bh	-13.7
0011010	1Ah	-5.6	1000011	43h	-9.7	1101100	6Ch	-13.8
0011011	1Bh	-5.7	1000100	44h	-9.8	1101101	6Dh	-13.9
0011100	1Ch	-5.8	1000101	45h	-9.9	1101110	6Eh	-14
0011101	1Dh	-5.9	1000110	46h	-10	1101111	6Fh	-14.1
0011110	1Eh	-6	1000111	47h	-10.1	1110000	70h	-14.2
0011111	1Fh	-6.1	1001000	48h	-10.2	1110001	71h	-14.3
0100000	20h	-6.2	1001001	49h	-10.3	1110010	72h	-14.4
0100001	21h	-6.3	1001010	4Ah	-10.4	1110011	73h	-14.5
0100010	22h	-6.4	1001011	4Bh	-10.5	1110100	74h	-14.6
0100011	23h	-6.5	1001100	4Ch	-10.6	1110101	75h	-14.7
0100100	24h	-6.6	1001101	4Dh	-10.7	1110110	76h	-14.8
0100101	25h	-6.7	1001110	4Eh	-10.8	1110111	77h	-14.9
0100110	26h	-6.8	1001111	4Fh	-10.9	1111000	78h	-15
0100111	27h	-6.9	1010000	50h	-11	other		-15
0101000	28h	-7	1010001	51h	-7.1			

Notes:

1. VSP_0/VSN_0 voltage output is ±15 V fixed value.
2. When switching Mode0 or Mode1,the voltage output is:
   Mode0: VSP_0(+15) / VSN_0 (-15) / VSPL_0 (+3~+15)
   Mode1: VSP_1(+3 ~ +15) / VSN_1(-3 ~ -15) / VSPL_1(+3 ~ +15)

	Mode0	Mode1
VSP	VSP_0(+15)	VSP_1(+3~+15)
VSN	VSN_0(-15)	VSN_1(-3~-15)
VSPL	VSPL_0(+3~+15)	VSPL_1(+3~+15)

3. If gate voltage is set to +/-15v, +/-10v, IC will auto correct source voltage as follows
   I. VGP- VSP_0 / VSPL_0 / VSP_1 / VSPL_1 >= 2v
   II. VGN- VSN_0 / VSN_1 >= -2v
   For example:

	symbol	Voltage setting	Real Voltage
Voltage	VGP	10v	+10v
	VGN	10v	-10v
	VSP_0	+15v	+8v
	VSN_0	-15v	-8v
	VSP_1	+5v	+5v
	VSN_1	-5v	-5v
	VSPL	+15v	+8v
	VCOMH	+15v+(-2v)	+8v +(-2v)
	VCOML	-15v+(-2v)	-8v +(-2v)
	VCOMDC	-2v	-2v

4. Voltage setting limit: VSP_0 ≥ VSPL_0 , VSP_1 ≥ VSPL_1

Restriction

R02H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
POF	W	0	0	0	0	0	0	0	1	0	02H
1st Parameter	W	1	-	-	-	-	-	-	-	EDSE	00

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

- After power off command, driver will power off base on power off sequence.
- After power off command, BUSY_N signal will drop from high to low. When finish the power off sequence, BUSY_N singal will rise from low to high.
- Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off.
- SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

1st parameter

Bit	Name	Description
0	EDSE	EPD Discharge Trigger 0 : Disable EPD discharge (default) 1 : Enable EPD discharge

Restriction: This command only active when BUSY_N = "1".

R03H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PFS	W	0	0	0	0	0	0	0	1	1	03H
1st Parameter	W	1	-		T_VDPG_OFF [1:0]		-		T_VDS_OFF [1:0]		00h
2nd Parameter	W	1	VGP_LEN[3:0]				VGP_EXT[3:0]				54h
3rd Parameter	W	1	XON_DLY[3:0]				XON_LEN[3:0]				44h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

1st Parameter:

Bit	Name	Description
1-0	T_VDS_OFF	Power off sequence of VSP /VSN 00: 20 ms (default) 01: 40 ms 10: 60 ms 11: 80 ms
5-4	T_VDPG_OFF	Power off sequence of VGP and VGN 00: 20 ms (default) 01: 40 ms 10: 60 ms 11: 80 ms

GDISPLAY

2nd Parameter

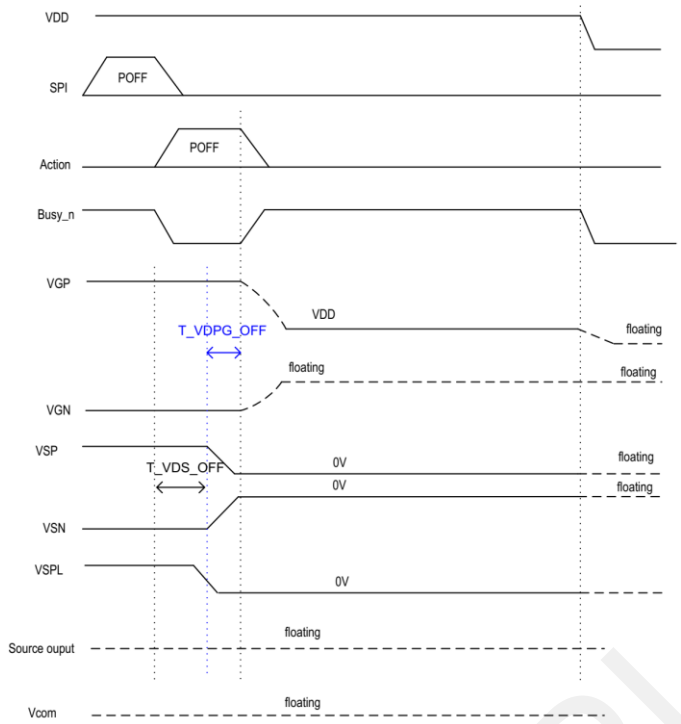
Bit	Name	Description
1-0	VGP_EXT	VGP extension time 0000: 0 ms 0001: 500 ms 0010: 1000 ms 0011: 1500 ms 0100: 2000 ms (default) 0101: 2500 ms 0110: 3000 ms 0111: 3500 ms 1000: 4000 ms 1001: 4500 ms 1010: 5000 ms 1011: 5500 ms 1100: 6000 ms 1101: 6500 ms
7-4	VGP_LEN	When power off, the length of time VGP stay 10V 0000: 0 ms 0001: 500 ms 0010: 1000 ms 0011: 1500 ms 0100: 2000 ms 0101: 2500 ms (default) 0110: 3000 ms 0111: 3500 ms 1000: 4000 ms 1001: 4500 ms 1010: 5000 ms 1011: 5500 ms 1100: 6000 ms 1101: 6500 ms

3rd Parameter:

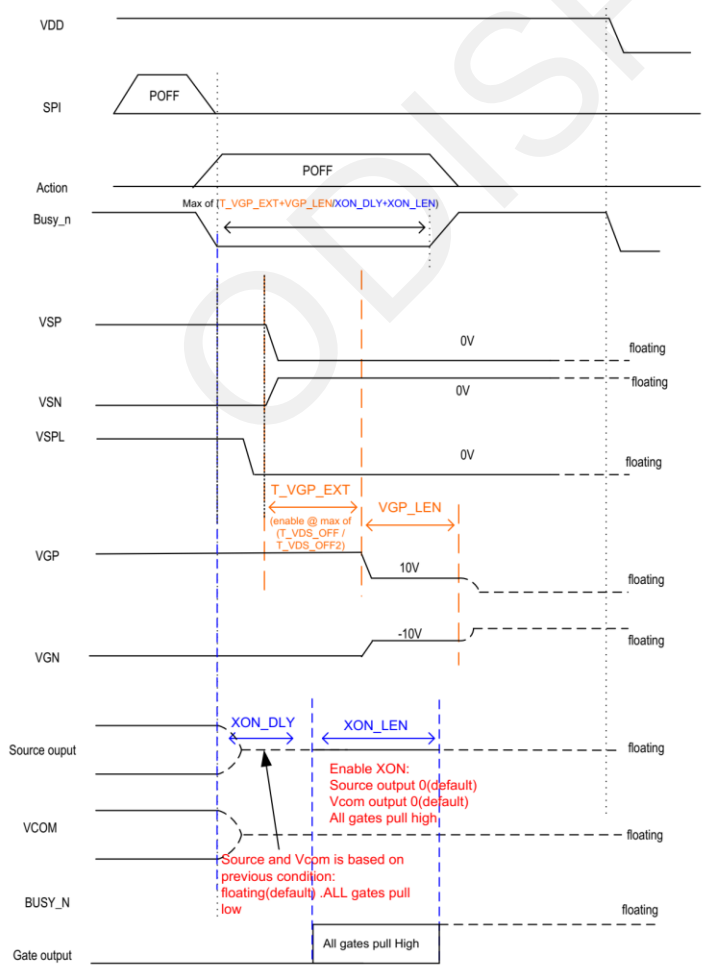
Bit	Name	Description
3-0	XON_LEN	XON enable time 0000: 0 ms 0001: 500 ms 0010: 1000 ms 0011: 1500 ms 0100: 2000 ms (default) 0101: 2500 ms 0110: 3000 ms 0111: 3500 ms 1000: 4000 ms 1001: 4500 ms 1010: 5000 ms 1011: 5500 ms 1100: 6000 ms
7-4	XON_DLY	XON delay time 0000: 0 ms 0001: 500 ms 0010: 1000 ms 0011: 1500 ms 0100: 2000 ms (default) 0101: 2500 ms 0110: 3000 ms 0111: 3500 ms 1000: 4000 ms 1001: 4500 ms 1010: 5000 ms 1011: 5500 ms 1100: 6000 ms

GOODISPLAY

Power off Sequence(R02h=00)



Power off Sequence(R02h=01)



Restriction	

GODISPLAY

R04H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PON	W	0	0	0	0	0	0	1	0	0	04H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ● After power on command, driver will power on base on power on sequence. ● After power on command, BUSY_N signal will drop from high to low. When finishing the power on sequence, BUSY_N signal will rise from low to high.
Restriction	This command only active when BUSY_N = "1".

R06H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
BTST	W	0	0	0	0	0	0	1	1	0	06H
1st Parameter	W	1	-	-	-	-	PHB_SFT [1:0]		PHA_SFT [1:0]		17h
2nd Parameter	W	1	-	-	PHA_ON [5:0]						02h
3rd Parameter	W	1	-	-	PHA_OFF [5:0]						07h
4th Parameter	W	1	-	-	PHB_ON [5:0]						02h
5th Parameter	W	1	-	-	PHB_OFF [5:0]						07h
6th Parameter	W	1	-	-	PHC_ON [5:0]						02h
7th Parameter	W	1	-	-	PHC_OFF [5:0]						07h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command define as follows:

1st Parameter:

Bit	Name	Description
1-0	PHA_SFT	Soft start period of phase A: 00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS
3-2	PHB_SFT	Soft start period of phase B: 00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS

	Bit[5:0]	Description	Bit[5:0]	Description	Bit[5:0]	Description
Driving strength of PHA_ON & PHB_ON & PHC_ON	000000	strength1	010110	strength23	101100	strength45
	000001	strength2	010111	strength24	101101	strength46
	000010	strength3	011000	strength25	101110	strength47
	000011	strength4	011001	strength26	101111	strength48
	000100	strength5	011010	strength27	110000	strength49
	000101	strength6	011011	strength28	110001	strength50
	000110	strength7	011100	strength29	110010	strength51
	000111	strength8	011101	strength30	110011	strength52
	001000	strength9	011110	strength31	110100	strength53
	001001	strength10	011111	strength32	110101	strength54
	001010	strength11	100000	strength33	110110	strength55
	001011	strength12	100001	strength34	110111	strength56
	001100	strength13	100010	strength35	111000	strength57
	001101	strength14	100011	strength36	111001	strength58
	001110	strength15	100100	strength37	111010	strength59
	001111	strength16	100101	strength38	111011	strength60
	010000	strength17	100110	strength39	111100	strength61
	010001	strength18	100111	strength40	111101	strength62
	010010	strength19	101000	strength41	111110	strength63
	010011	strength20	101001	strength42	111111	strength64
	010100	strength21	101010	strength43		
	010101	strength22	101011	strength44		

Description		Bit[5:0]	Description	Bit[5:0]	Description	Bit[5:0]	Description
	Minimum OFF time setting of PHA_OFF & PHB_OFF & PHC_OFF	000000	Period1	010110	Period23	101100	Period45
		000001	Period2	010111	Period24	101101	Period46
		000010	Period3	011000	Period25	101110	Period47
		000011	Period4	011001	Period26	101111	Period48
		000100	Period5	011010	Period27	110000	Period49
		000101	Period6	011011	Period28	110001	Period50
		000110	Period7	011100	Period29	110010	Period51
		000111	Period8	011101	Period30	110011	Period52
		001000	Period9	011110	Period31	110100	Period53
		001001	Period10	011111	Period32	110101	Period54
		001010	Period11	100000	Period33	110110	Period55
		001011	Period12	100001	Period34	110111	Period56
		001100	Period13	100010	Period35	111000	Period57
		001101	Period14	100011	Period36	111001	Period58
		001110	Period15	100100	Period37	111010	Period59
		001111	Period16	100101	Period38	111011	Period60
		010000	Period17	100110	Period39	111100	Period61
		010001	Period18	100111	Period40	111101	Period62
		010010	Period19	101000	Period41	111110	Period63
		010011	Period20	101001	Period42	111111	Period64
		010100	Period21	101010	Period43		
		010101	Period22	101011	Period44		
Restriction							

R07H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSLP	W	0	0	0	0	0	0	1	1	1	07H
1st Parameter	W	1	1	0	1	0	0	1	0	1	A5h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: After this command is transmitted, the chip would enter the deep-sleep mode to save power. The deep sleep mode would return to standby by hardware reset. The only one parameter is a check code, the command would be excited if check code = 0xA5.
Restriction	This command only active when BUSY_N = "1".

R10H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM1	W	0	0	0	0	1	0	0	0	0	10H
1st Parameter	W	1	Pixel1		Pixel2		Pixel3		Pixel4		00h
2nd Parameter	W	1	: Pixel(n-3)		: Pixel(n-2)		: Pixel(n-1)		: Pixel(n)		00h
…	W	1									00h
Mth Parameter	W	1	Pixel1		Pixel2		Pixel3		Pixel4		00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

The command define as follows:

The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 12H. Then chip will start to send data/VCOM for panel.

Pixel [1~n][1:0]: 2-bit/pixel

Image Data	DDX=1(default)		DDX=0	
Pixel[1:0]	Gray level select	IP output LUT select	Gray level select	IP output LUT select
00b	Gray0	ogray00	Gray3	ogray03
01b	Gray1	ogray01	Gray2	ogray02
10b	Gray2	ogray02	Gray1	ogray01
11b	Gray3	ogray03	Gray0	ogray00

Restriction

R12H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DRF	W	0	0	0	0	1	0	0	1	0	12H
1st Parameter	W	1	-	-	-	-	-	-	-	AC/DC VCOM	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : While users send this command, driver will refresh display (data/VCOM) base on SRAM data and LUT. **AC/DC VCOM:** **0: AC VCOM, VCOM will follow LUTC when updating image. (default)** 1: DC VCOM, VCOM will always be VCOMDC when updating image After display refresh command, BUSY_N signal will become "0"
Restriction	This command only actives when BUSY_N = "1"

R17H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
Auto Sequence	W	0	0	0	0	1	0	1	1	1	17H
1st Parameter	W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	A5h

Description	The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP. AUTO (0x17) + Code(0xA5) = (PON→DRF→POF) AUTO (0x17) + Code(0xA7) = (PON→DRF→POF→DSLP)
Restriction	This command only actives when BUSY_N = "1".

R30H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PLL	W	0	0	0	1	1	0	0	0	0	30H
1st Parameter	W	1	-	-	-	-	Dyna	FR[2:0]			02h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

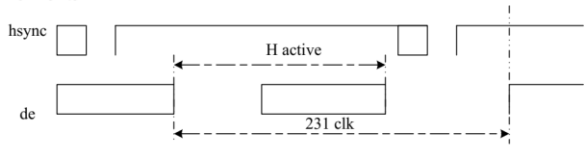
The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

bit3	Dynamic frame rate
0	Disable(default)
1	Enable

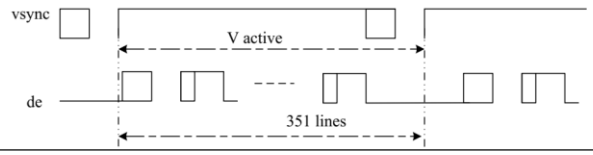
FR[2:0]	Frame rate
000	12.5 Hz
001	25 Hz
010	50 Hz(default)
011	65 Hz
100	75 Hz
101	85 Hz
110	100 Hz
111	120 Hz

remark

-Horizental



-Vertical



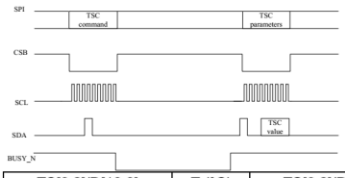
Restriction

R40H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSC	W	0	0	1	0	0	0	0	0	0	40H
1st Parameter	R	1	D10/TS[9]	D9/TS[8]	D8/TS[7]	D7/TS[6]	D6/TS[5]	D5/TS[4]	D4/TS[3]	D3/TS[2]	-
2nd Parameter	R	1	D2/TS[1]	D1/ TS[0]	D0	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command define as follows:
This command indicates the temperature value.
If R41H(TSE) bit7 set to 0, this command reads internal temperature sensor value.
If R41H(TSE) bit7 set to 1, this command reads external (LM75) temperature sensor value



TS[9:2]/D[10:3]	T (°C)	TS[9:2]/D[10:3]	T (°C)	TS[9:2]/D[10:3]	T (°C)
11100111	-25	00000000	0	00011001	25
11101000	-24	00000001	1	00011010	26
11101001	-23	00000010	2	00011011	27
11101010	-22	00000011	3	00011100	28
11101011	-21	00000100	4	00011101	29
11101100	-20	00000101	5	00011110	30
11101101	-19	00000110	6	00011111	31
11101110	-18	00000111	7	00100000	32
11101111	-17	00001000	8	00100001	33
11110000	-16	00001001	9	00100010	34
11110001	-15	00001010	10	00100011	35
11110010	-14	00001011	11	00100100	36
11110011	-13	00001100	12	00100101	37
11110100	-12	00001101	13	00100110	38
11110101	-11	00001110	14	00100111	39
11110110	-10	00001111	15	00101000	40
11110111	-9	00010000	16	00101001	41
11111000	-8	00010001	17	00101010	42
11111001	-7	00010010	18	00101011	43
11111010	-6	00010011	19	00101100	44
11111011	-5	00010100	20	00101101	45
11111100	-4	00010101	21	00101110	46
11111101	-3	00010110	22	00101111	47
11111110	-2	00010111	23	00110000	48
11111111	-1	00011000	24	00110001	49

TS[1:0]	T (°C)
00	+0
01	+0.25
10	+0.5
11	+0.75

Restriction: This command only actives when BUSY_N = "1".

R41H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSE	W	0	0	1	0	0	0	0	0	1	41H
1st Parameter	W	1	TSE	-	TO[5]	TO[4]	TO[3]	TO[2]	TO[1]	TO[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the driver IC temperature sensor enable and calibration function.

Reserve one temperature offset TO[3:0] for calibration
1. TO[3]: mean '+' or '-' , while 0 is '+' ; 1 is '-'
2. TO[2:0]: mean temperature offset value

Bit	Name	Description
3-0	TO[3:0]	Temperature level: 0000: +0°C (default) 0001: +0.5°C 0010: +1°C 0011: +1.5°C 0100: +2°C 0101: +2.5°C 0110: +3°C 0111: +3.5°C 1000: -4°C 1001: -3.5°C 1010: -3°C 1011: -2.5°C 1100: -2°C 1101: -1.5°C 1110: -1°C 1111: -0.5°C

5-4	TO[5:4]	0: +0.0℃ (default) 1: +0.25℃
7	TSE	Internal temperature sensor enable 0: Internal temperature sensor enable.(default) 1: Internal temperature sensor disable, using external temperature sensor.

Restriction: This command only actives after R04H(PON)

R50H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CDI	W	0	0	1	0	1	0	0	0	0	50H
1st Parameter	W	1	VBD[2]	VBD[1]	VBD [0]	DDX	CDI[3]	CDI[2]	CDI[1]	CDI[0]	97h

NOTE: "-" Don't care, can be set to VDD or GND level

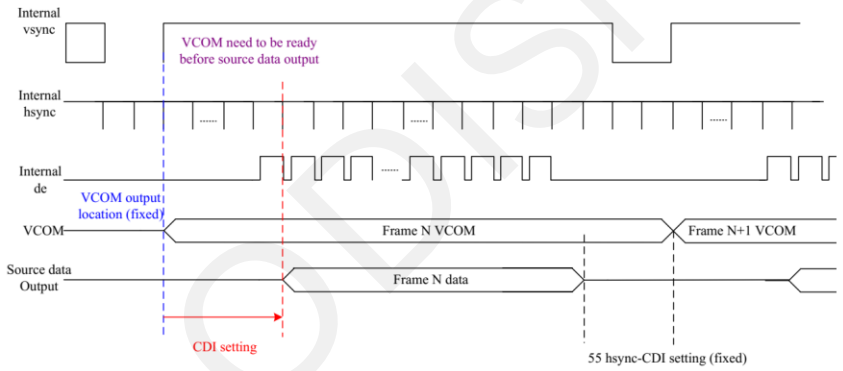
Description

-The command defines as:

1st Parameter:

CDI[1:0]: This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be keep (55hsync).

Bit	Name	Description
3-0	CDI[3:0]	Vcom and data interval 0000: 17 hsync 0001:16 hsync 0010:15 hsync 0011:14 hsync 0100:13 hsync 0101:12 hsync 0110:11 hsync 0111:10 hsync(default) 1000:9 hsync 1001:8 hsync 1010:7 hsync 1011:6 hsync 1100:5 hsync 1101:4 hsync 1110:3 hsync 1111:2 hsync



VBD[2:0]: Border data selection. (from LUT output by IP port border_w[1:0])

This register will make boarder pin output being mapped to a certain gray scale.

Bit 4	Bit7-5	Description	IP setting for Border LUT select
DDX	VBD[2:0]	Gray level	
0	000	Floating	N/A
	001	Gray3	border_buf=011
	010	Gray2	border_buf=010
	011	Gray1	border_buf=001
	100	Gray0	border_buf=000
1 (default)	000	Gray0	border_buf=000
	001	Gray1	border_buf=001
	010	Gray2	border_buf=010
	011	Gray3	border_buf=011
	100	Floating	N/A

Border output voltage level: The level selection is based on mapping LUT data.

Ex: Gray 1 waveform is mapping to 15V,without VCOM offset, the real output on Boarder pin shall be 15V.

Boarder output will follow FOPT definition being defined in R00h.

Restriction

GDDISPLAY

R51H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LPD	W	0	0	1	0	1	0	0	0	1	51H
1st Parameter	R	1	-	-	-	-	-	-	-	LPD	--

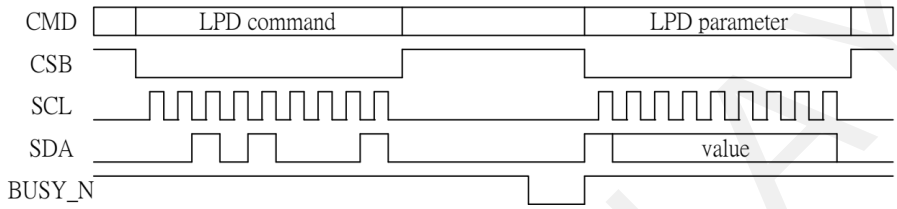
NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the input power condition. Host can read this data to understand the battery's condition.
When LPD="1", system input power is normal.
When LPD="0", system input power is lower (VDD<2.5v, which could be select in RE4H (LVSEL)).

1st Parameter:

Bit	Name	Description
0	LPD	0: Low power input 1: Normal status



Restriction

- This command only actives when BUSY_N = "1".

R61H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TRES	W	0	0	1	1	0	0	0	0	1	61H
1st Parameter	W	1	-	-	-	-	-	-	HRES(9)	HRES(8)	00h
2nd Parameter	W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	HRES(2)	0	0	00h
3rd Parameter	W	1	-	-	-	-	-	-	VRES(9)	VRES(8)	00h
4th Parameter	W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command define as follows:
When using register:
Horizontal display resolution = HRES
Vertical display resolution = VRES

Channel disable calculation:
GD : First G active = G0; LAST active GD= first active +VRES[9:0] -1
SD : First active channel: =S0 ; LAST active SD= first active +HRES[9:2]*8-1

EX :200X384
GD: First G active = G0
LAST active GD= 0+384-1= 383; (G383)
SD : First active channel: =S0
LAST active SD=0+50*4-1=199; (S199)
R61H = 00h,C8h, 01h, 80h (解析度直接轉 16 進制即為設定值)

Note: Only supports source 200.ch for source 184ch. above

Restriction

R65H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
GSST	W	0	0	1	1	0	0	1	0	1	65H
1st Parameter	W	1	-	-	-	-	-	-	S_start[9]	S_start[8]	00h
2nd Parameter	W	1	S_start[7]	S_start[6]	S_start[5]	S_start[4]	S_start[3]	S_start[2]	-	-	00h
3rd Parameter	W	1	-	-	-	-	-	-	G_start[9]	G_start[8]	00h
4th Parameter	W	1	G_start[7]	G_start[6]	G_start[6]	G_start[4]	G_start[3]	G_start[2]	G_start[1]	G_start[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: 1.S_Start [9:2] describe which source output line is the first date line 2.G_Start[9:0] describe which gate line is the first scan line
Restriction	

R70H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
REV	W	0	0	1	1	1	0	0	0	0	70H
1st Parameter	R	1	0	0	0	0	0	0	1	1	03h
2nd Parameter	R	1	0	0	0	0	0	0	1	0	02h
3rd Parameter	R	1	0	0	0	0	0	0	0	1	01h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: The LUT_REV is read from: 1st & 2nd & 3rd Parameter :
Restriction	

Bit	Description
3-0	CHIP_REV

R80H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
AMV	W	0	1	0	0	0	0	0	0	0	80H
1st Parameter	W	1	-	-	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	10h

NOTE: "-" Don't care, can be set to VDD or GND level

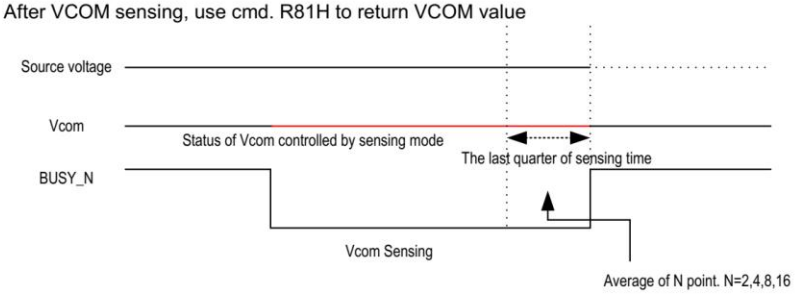
Description

-The command defines as:
This command indicates the IC status. Host can read this data to understand the IC status.

1st Parameter:

Bit	Name	Description
0	AMVE	AMVE: Auto Measure Vcom Setting 0: Auto measure VCOM disable (default) 1: Auto measure VCOM enable
1	AMV	AMV: Analog signal 0:Get Vcom value from R81h(default) 1:Get Vcom value in analog signal
2	AMVS	AMVS: setting for Source output of AMV 0: Source output 0V during Auto Measure VCOM period. (default) 1: Source output VSPL_0 during Auto Measure VCOM period.
3	XON	XON: setting for all Gate ON of AMV 0: Gate normally scan during Auto Measure VCOM period. (default) 1: All Gate ON during Auto Measure VCOM period.
5-4	AMVT[1:0]	The sensing time of VCOM detection 00: 5s (default) 01: 10s 10: 15s 11: 20s

After VCOM sensing, use cmd. R81H to return VCOM value



Note:
1.VCOM設定至最小0V(R82h=80h)
2.外部穩壓電容floating

Restriction: This command only actives when BUSY_N = "1".

R81H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VV	W	0	1	0	0	0	0	0	0	1	81H
1st Parameter	R	1	-	-	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	--

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command could get the VCOM value

1st Parameter:

Bit	Name	Description
6-0	VV[6:0]	

VCOM value

VCOM[6:0]		Voltage(V)	VCOM[6:0]		Voltage(V)	VCOM[6:0]		Voltage(V)
0000000	00h	0	0011100	1Ch	-1.4	0111000	38h	-2.8
0000001	01h	-0.05	0011101	1Dh	-1.45	0111001	39h	-2.85
0000010	02h	-0.1	0011110	1Eh	-1.5	0111010	3Ah	-2.9
0000011	03h	-0.15	0011111	1Fh	-1.55	0111011	3Bh	-2.95
0000100	04h	-0.2	0100000	20h	-1.6	0111100	3Ch	-3
0000101	05h	-0.25	0100001	21h	-1.65	0111101	3Dh	-3.05
0000110	06h	-0.3	0100010	22h	-1.7	0111110	3Eh	-3.1
0000111	07h	-0.35	0100011	23h	-1.75	0111111	3Fh	-3.15
0001000	08h	-0.4	0100100	24h	-1.8	1000000	40h	-3.2
0001001	09h	-0.45	0100101	25h	-1.85	1000001	41h	-3.25
0001010	0Ah	-0.5	0100110	26h	-1.9	1000010	42h	-3.3
0001011	0Bh	-0.55	0100111	27h	-1.95	1000011	43h	-3.35
0001100	0Ch	-0.6	0101000	28h	-2	1000100	44h	-3.4
0001101	0Dh	-0.65	0101001	29h	-2.05	1000101	45h	-3.45
0001110	0Eh	-0.7	0101010	2Ah	-2.1	1000110	46h	-3.5
0001111	0Fh	-0.75	0101011	2Bh	-2.15	1000111	47h	-3.55
0010000	10h	-0.8	0101100	2Ch	-2.2	1001000	48h	-3.6
0010001	11h	-0.85	0101101	2Dh	-2.25	1001001	49h	-3.65
0010010	12h	-0.9	0101110	2Eh	-2.3	1001010	4Ah	-3.7
0010011	13h	-0.95	0101111	2Fh	-2.35	1001011	4Bh	-3.75
0010100	14h	-1	0110000	30h	-2.4	1001100	4Ch	-3.8
0010101	15h	-1.05	0110001	31h	-2.45	1001101	4Dh	-3.85
0010110	16h	-1.1	0110010	32h	-2.5	1001110	4Eh	-3.9
0010111	17h	-1.15	0110011	33h	-2.55	1001111	4Fh	-3.95
0011000	18h	-1.2	0110100	34h	-2.6	1010000	50h	-4
0011001	19h	-1.25	0110101	35h	-2.65	other		-4
0011010	1Ah	-1.3	0110110	36h	-2.7			
0011011	1Bh	-1.35	0110111	37h	-2.75			

Restriction

R82H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VDCS	W	0	1	0	0	0	0	0	1	0	82H
1st Parameter	W	1	MTP_VCM	VDCS[6]	VDCS[5]	VDCS [4]	VDCS [3]	VDCS [2]	VDCS [1]	VDCS [0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command set the VCOM DC value. Driver will base on this value for VCM_DC.
1st Parameter:
1st Parameter:

Bit	Name	Description

VCOM value

VCOM[6:0]		Voltage(V)	VCOM[6:0]		Voltage(V)	VCOM[6:0]		Voltage(V)
0000000	00h	0(default)	0011100	1Ch	-1.4	0111000	38h	-2.8
0000001	01h	-0.05	0011101	1Dh	-1.45	0111001	39h	-2.85
0000010	02h	-0.1	0011110	1Eh	-1.5	0111010	3Ah	-2.9
0000011	03h	-0.15	0011111	1Fh	-1.55	0111011	3Bh	-2.95

	6-0	VDCS[6:0]	0000100	04h	-0.2	0100000	20h	-1.6	0111100	3Ch	-3
			0000101	05h	-0.25	0100001	21h	-1.65	0111101	3Dh	-3.05
			0000110	06h	-0.3	0100010	22h	-1.7	0111110	3Eh	-3.1
			0000111	07h	-0.35	0100011	23h	-1.75	0111111	3Fh	-3.15
			0001000	08h	-0.4	0100100	24h	-1.8	1000000	40h	-3.2
			0001001	09h	-0.45	0100101	25h	-1.85	1000001	41h	-3.25
			0001010	0Ah	-0.5	0100110	26h	-1.9	1000010	42h	-3.3
			0001011	0Bh	-0.55	0100111	27h	-1.95	1000011	43h	-3.35
			0001100	0Ch	-0.6	0101000	28h	-2	1000100	44h	-3.4
			0001101	0Dh	-0.65	0101001	29h	-2.05	1000101	45h	-3.45
			0001110	0Eh	-0.7	0101010	2Ah	-2.1	1000110	46h	-3.5
			0001111	0Fh	-0.75	0101011	2Bh	-2.15	1000111	47h	-3.55
			0010000	10h	-0.8	0101100	2Ch	-2.2	1001000	48h	-3.6
			0010001	11h	-0.85	0101101	2Dh	-2.25	1001001	49h	-3.65
			0010010	12h	-0.9	0101110	2Eh	-2.3	1001010	4Ah	-3.7
			0010011	13h	-0.95	0101111	2Fh	-2.35	1001011	4Bh	-3.75
			0010100	14h	-1	0110000	30h	-2.4	1001100	4Ch	-3.8
			0010101	15h	-1.05	0110001	31h	-2.45	1001101	4Dh	-3.85
			0010110	16h	-1.1	0110010	32h	-2.5	1001110	4Eh	-3.9
			0010111	17h	-1.15	0110011	33h	-2.55	1001111	4Fh	-3.95
			0011000	18h	-1.2	0110100	34h	-2.6	1010000	50h	-4
			0011001	19h	-1.25	0110101	35h	-2.65	other	-4	
			0011010	1Ah	-1.3	0110110	36h	-2.7			
			0011011	1Bh	-1.35	0110111	37h	-2.75			

	7	MTP_VCM	Follow MTP VCOM value in MTP mode 0: From the setting of MTP (default) 1:From the setting of register
Restriction			

R83H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PTL	W	0	1	0	0	0	0	0	1	1	83H
1st Parameter	W	1	-	-	-	-	-	-	HRST[9]	HRST[8]	00h
2nd Parameter	W	1	HRST[7]	HRST[6]	HRST[5]	HRST[4]	HRST[3]	HRST[2]	-	-	00h
3rd Parameter	W	1	-	-	-	-	-	-	HRED[9]	HRED[8]	00h
4th Parameter	W	1	HRED[7]	HRED[6]	HRED[5]	HRED[4]	HRED[3]	HRED[2]	-	-	00h
5th Parameter	W	1	-	-	-	-	-	-	VRST[9]	VRST[8]	00h
6th Parameter	W	1	VRST[7]	VRST[6]	VRST[5]	VRST[4]	VRST[3]	VRST[2]	VRST[1]	VRST[0]	00h
7th Parameter	W	1	-	-	-	-	-	-	VRED[9]	VRED[8]	00h
8th Parameter	W	1	VRED[7]	VRED[6]	VRED[5]	VRED[4]	VRED[3]	VRED[2]	VRED[1]	VRED[0]	00h
9th Parameter	W	1	-	-	-	-	-	-	-	PMODE	00h

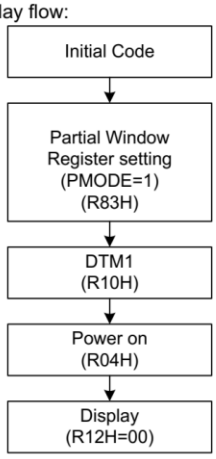
NOTE: "-" Don't care, can be set to VDD or GND level

Description

-This command sets partial window.

Name	Description
HRST[9:2]	Horizontal start address
HRED[9:2]	Horizontal end address. HRED must be greater than HRST.
VRST[9:0]	Vertical start address.
VRED[9:0]	Vertical end address. VRED must be greater than VRST.
PMODE	0: disable partial mode(default) 1: enable partial mode

Note:
No matter HRST[1:0] ,HRST[9:8],HRED[9:8],VRST[9],VRED[9] value being filled, it's always be 00b.
No matter HRED[1:0] value being filled, it's always be 11b.

	Gates scan both inside and outside of the partial window. Partial display flow: 
Restriction	

R90H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PGM	W	0	1	0	1	0	0	0	0	0	A0H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is issued, the chip would enter the program mode. The mode would return to standby by hardware reset.
Restriction	This command only actives when BUSY_N = "1".

R91H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
APG	W	0	1	0	0	1	0	0	0	1	91H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is transmitted, the programming state machine would be activated.
Restriction	The BUSY flag would change state from 0 to 1 while the programming is completed.

R92H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
RMTP	W	0	1	0	0	1	0	0	1	0	92H
1st Parameter	R	1	Dummy								-
2nd Parameter	R	1	The data of address 0x000 in the MTP								-
3rd Parameter	R	1	The data of address 0x001 in the MTP								-
4th Parameter	R	1	:								-
5th Parameter	R	1	The data of address (n-1) in the MTP								-
6th~(m-1)th Parameter	R	1	.....								-
mth Parameter	R	1	The data of address (n) in the MTP								-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: The command is used for reading the content of MTP for checking the data of programming. The value of (n) is depending on the amount of programmed data, the max address = 0x17FF.
Restriction	This command only actives when BUSY_N = "1".

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R9FH	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
RMRB	W	0	1	0	0	1	1	1	1	1	9FH
1st Parameter	R	1	Dummy								-
2nd Parameter	R	1	The data of address 0x16F7 in the MTP								00h
3rd Parameter	R	1	:								00h
:	R	1	:								00h
97th Parameter	R	1	:								00h
98th Parameter	R	1	:								00h
101th Parameter	R	1	The data of address 0x175A in the MTP								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: The command is used for reading the content of MTP Reserved Byte for checking the data of programming. This command could read these information from MTP directly.
Restriction	This command only actives when BUSY_N = "1".

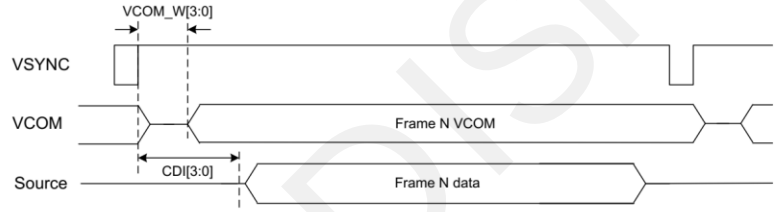
RE3H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWS	W	0	1	1	1	0	0	0	1	1	E3H
1st Parameter	W	1	VCOM_W[3:0]				SD_W[3:0]				00h

NOTE: "-" Don't care, can be set to VDD or GND level

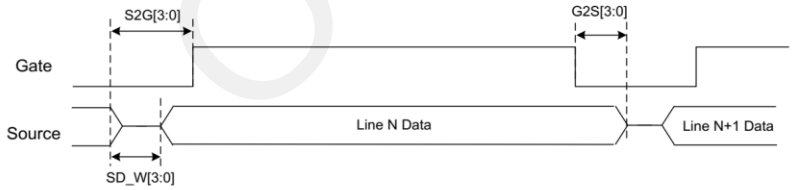
Description

- This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W: VCOM power saving width (unit = line period)



SD_W: Source power saving width (unit = 660nS)



Restriction

RE4H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LVSEL	W	0	1	1	1	0	0	1	0	0	E4H
1st Parameter	W	1	-	-	-	-	-	-	LVD_SEL[1:0]		03h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

LVD_SEL[1:0]: Low Power Voltage Selection

LVD_SEL[1:0]	LVD value
00	< 2.2 V
01	< 2.3 V
10	< 2.4 V
11	< 2.5 V (default)

Restriction

8. Handling, Safety and Environment Requirements

Warning	
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.	
Caution	
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module. Disassembling the display module can cause permanent damage and invalidates the warranty agreements. Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.	
Data sheet status	
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134).Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

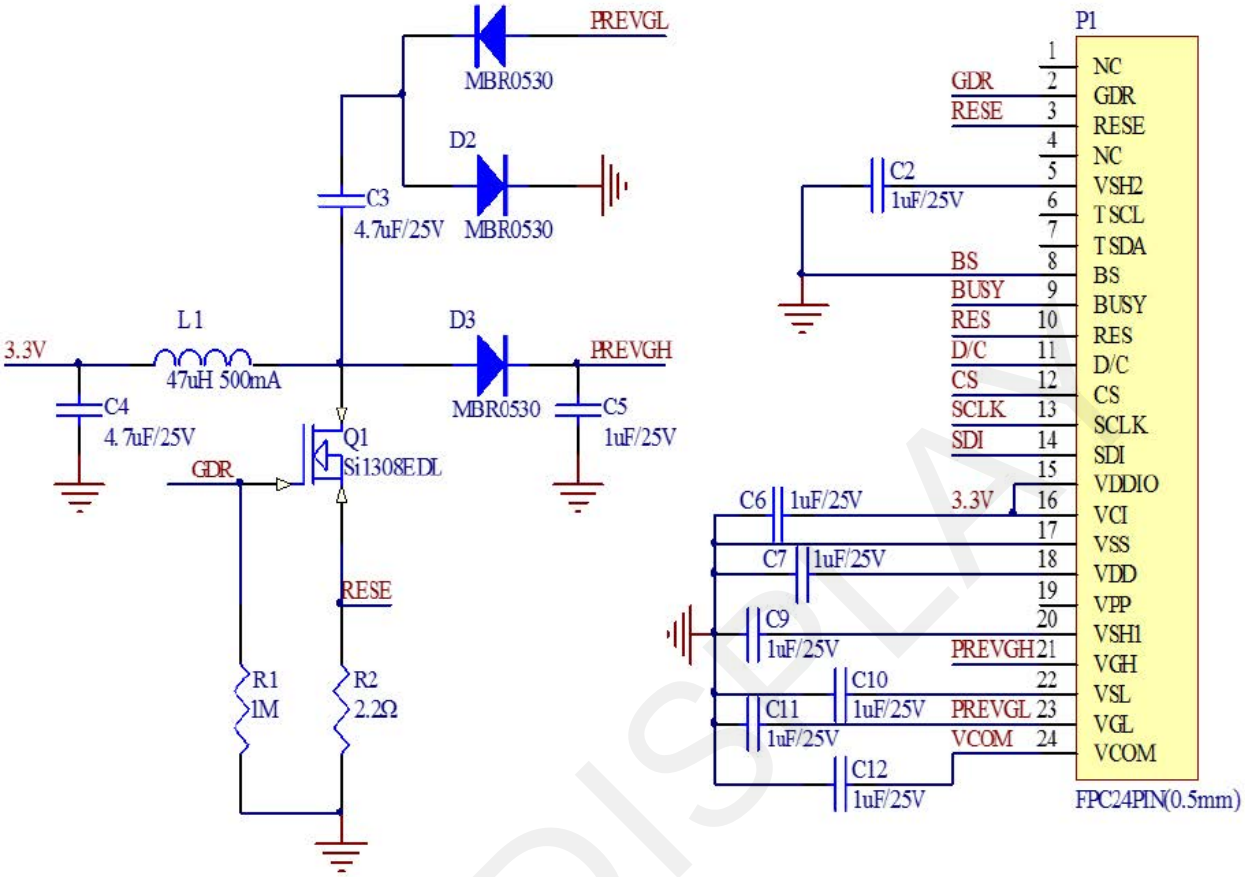
9. Reliability test

NO	Test items	Test condition
1	Low-Temperature Storage	T = -25 ℃, 240 h Test in white pattern
2	High-Temperature Storage	T=60° C， RH=35%， 240h Test in white pattern
3	High-Temperature Operation	T=40° C， RH=35%， 240h
4	Low-Temperature Operation	0° C， 240h
5	High-Temperature, High-Humidity Operation	T=40° C， RH=80%， 240h
6	High Temperature, High Humidity Storage	T=50° C， RH=90%, 240h Test in white pattern
7	Temperature Cycle	1 cycle:[-25℃ 30min]→[+60℃ 30 min] : 50 cycles Test in white pattern
8	UV exposure Resistance	765W/m ²for 168hrs,40 ℃ Test in white pattern
9	ESD Gun	Air+/-15KV;Contact+/-8KV (Test finished product shell, not display only) Air+/-8KV;Contact+/-6KV (Naked EPD display, no including IC and FPC area) Air+/-4KV;Contact+/-2KV (Naked EPD display, including IC and FPC area)

Note: Put in normal temperature for 1hour after test finished, display performance is ok.

ODISPLAY

10. Typical Application Circuit



Part Name	Requirements for spare part
C1—C12	0603/0805; X5R/X7R;Voltage Rating:≥25V
R1、R2	0603/0805;1% variation,≥0.05W
D1—D3	MBR0530: 1)Reverse DC Voltage≥30V 2)Io≥500mA 3)Forward voltage ≤430mV
Q1	Si1308EDL:1)Drain-Source breakdown voltage≥30V 2)Vgs(th)≤1.5V 3)Rds(on)≤400mΩ
L1	refer to NR3015: Io=500mA(max)
P1	24pins,0.5mm pitch

11. Matched Development Kit

Our Development Kit designed for SPI E-paper Display aims to help users to learn how to use E-paper Display more easily. It can refresh black-white E-paper Display, three-color (black, white and red/Yellow) E-paper Display and four-color(black, white, red and yellow) Good Display 's E-pa per Display. And it is also added the functions of USB serial port, FLASH chip, font chip, current detection ect.
Development Kit consists of the development board and the pinboard.

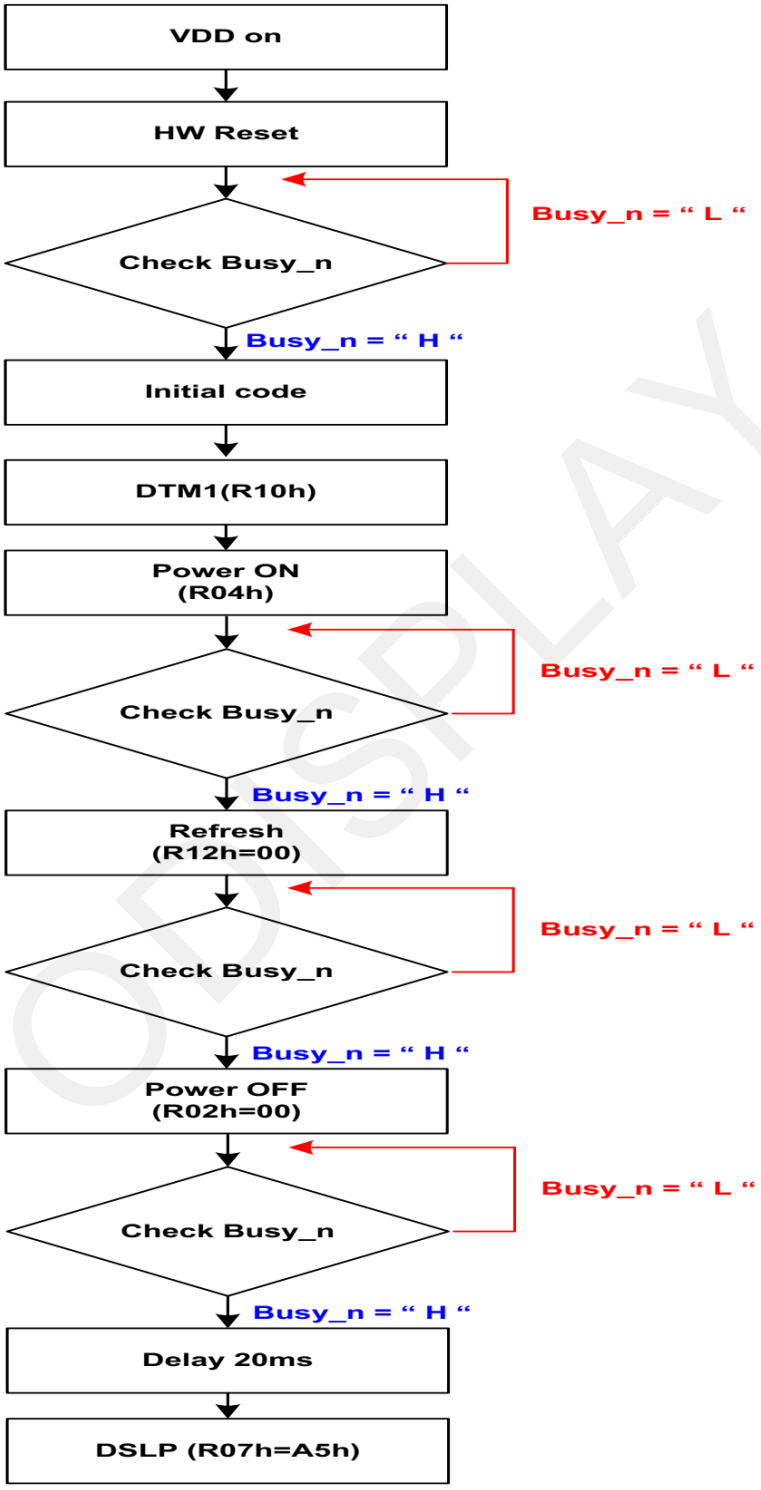
Supported development platforms include STM32, ESP32, ESP8266, Arduino UNO, etc. More details, please click to the following links:

STM32	https://www.good-display.com/product/219.html
ESP32	https://www.good-display.com/product/338.html
ESP8266	https://www.good-display.com/product/220.html
Arduino UNO	https://www.good-display.com/product/222.html

GODISPLAY

12. Typical Operating Sequence

12.1 Normal Operation Flow

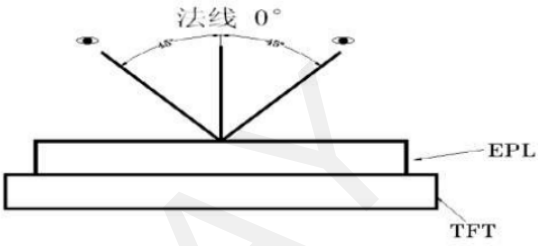


GDDISPLAY

13. Inspection method and condition

13. 1 Inspection condition

Item	Condition
Illuminance	800~1500 lux
Temperature	22℃±3℃
Humidity	55±10 %RH
Distance	≥30cm
Angle	Vertical fore and aft 45
Inspection method	By eyes

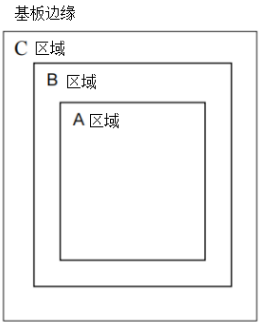


13. 2 Zone definition

A Zone: Active area

B Zone: Border zone

C Zone: From B zone edge to panel edge



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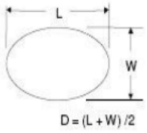
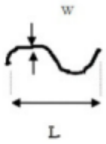
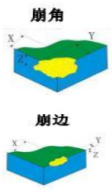
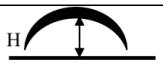
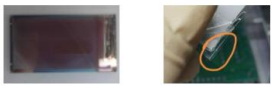
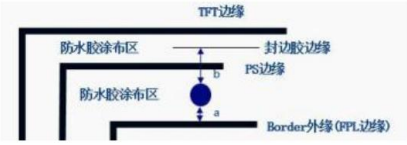
13. 3 General inspection standards for products

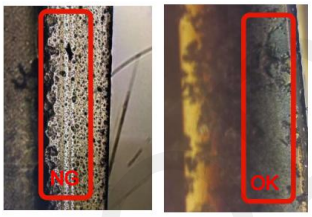
13.3.1 Appearance inspection standard

Inspection item		Figure		A zone inspection standard	B/C zone	Inspection method	MAJ/ MIN
Spot defects	Spot defects such as dot, foreign matter, air bubble, and dent etc.	Diameter D=(L+W)/2 (L-length、W-width) Measuring method shown in the figure below 	The distance between the two spots should not be less than 10mm	7.5"-13.3"Module（Not include 7.5"）： D＞1mm N=0 0.5＜D≤0.8 N≤4 D≤0.5 Ignore 0.8＜D≤1 N≤2 4.2"-7.5"Module（Not include 4.2"）： D＞0.5 N=0 0.4＜D≤0.5 N≤2 D≤0.25 Ignore 0.25＜D≤0.4 N≤4 Module below 4.2"： D＞0.5 N=0 0.4＜D≤0.5 N≤1 D≤0.25 Ignore 0.25＜D≤0.4 N≤4 0.1mm＜D≤0.25 N≤3/cm²	Foreign matter D≤1mm Pass	Check by eyes Film gauge	MIN

Inspection item		Figure		A zone inspection standard	B/C zone	Inspection method	MAJ/ MIN
Line defects	Line defects such as scratch, hair etc.	L-Length，W-Width, (W/L)＜1/4 Judged by line， (W/L)≥1/4 Judged by dot 	The distance between the two lines should not be less than 5mm	7.5"-13.3"Module（Not include 7.5"）： L＞10mm,N=0 W＞0.8mm，N=0 5mm≤L≤10mm，0.5mm≤W≤0.8mm N≤2 L≤5mm，W≤0.5mm Ignore 4.2"-7.5"Module（Not include 4.2"）： L＞8mm,N=0 W＞0.2mm，N=0 2mm≤L≤8mm，0.1mm≤W≤0.2mm N≤4 L≤2mm，W≤0.1mm Ignore Module below 4.2"： L＞5mm,N=0 W＞0.2mm，N=0 2mm≤L≤5mm，0.1mm≤W≤0.2mm N≤4 L≤2mm，W≤0.1mm Ignore	Ignore	Check by eyes Film gauge	MIN

Inspection item		Figure	Inspection standard	Inspection method	MAJ/ MIN
Panel chipping and crack defects	TFT panel chipping	X the length, Y the width, Z the chipping height, T the thickness of the panel 	Chipping at the edge： Module over 7.5"（Include 7.5"）： X≤ 6mm,Y≤1mm Z≤T N=3 Allowed Module below 7.5"(Not include 7.5")： X≤ 3mm,Y≤1mm Z≤T N=3 Allowed Chipping on the corner： IC sideX≤2mm Y≤2mm, Non-IC sideX≤1mm Y≤1mm . Allowed Note： Chipping should not damage the edge wiring. If it does not affect the display, allowed	Check by eyes、 Film gauge	MIN
	Crack		Crack at any zone of glass , Not allowed	Check by eyes、 Film gauge	MIN
	Burr edge		No exceed the positive and negative deviation of the outline dimensions X+Y≤0.2mm Allowed	Calliper	MIN
	Curl of panel	 Curl height	Curl height H≤Total panel length 1% Allowed	Check by eyes	MIN

Inspection item		Figure	Inspection standard	Inspection method	MAJ / MIN
PS defect	Water proof film		1 .Waterproof film damage, wrinkled, open edge, not allowed 2. Exceeding the edge of module(according to the lamination drawing) Not allowed 3. Edge warped exceeds height of technical file, not allowed	Check by eyes	MIN
RTV defect	Adhesive effect		Adhesive height exceeds the display surface, not allowed	Check by eyes	MIN
			1 .Overflow, exceeds the panel side edge, affecting the size, not allowed 2 .No adhesive at panel edge≤1mm, mo exposure of wiring, allowed 3. No adhesive at edge and corner1*1mm, no exposure of wiring, allowed		
			Protection adhesive, coverage width within W≤1.5mm, no break of adhesive, allowed		
	Adhesive re-fill		Dispensing is uniform, without obvious concave and breaking, bubbling and swell, not higher than the upper surface of the PS, and the diameter of the adhesive re-filling is not more than 8mm, allowed	Check by eyes	MIN
EC defect	Adhesive bubble		1、 Effective edge sealing area of hot melt products ≥1/2 edge sealing area; 2、Bubble a+b≥1/2 effective width, N≤3, spacing≥5mm , allowed No exposure of wiring, allowed	Check by eyes	MIN

Inspection item		Figure	Inspection standard	Inspection method	MAJ/ MIN
EC defect	Adhesive effect		1 .Overflow, exceeds the panel side edge, affecting the size, not allowed 2.No adhesive at panel edge≤1mm, mo exposure of wiring, allowed 3.No adhesive at edge and corner 1*1mm, no exposure of wiring, allowed 4. Adhesive height exceeds the display surface, not allowed	Visual, caliper	MIN
Silver dot adhesive defect	Silver dot adhesive		1、Single silver dot dispensing amount ≥1mm, allowed 2、One of the double silver dot dispensing amount is ≥1mm and the other has adhesive (no reference to 1mm) Allowed	Visual	MIN
			Silver dot dispensing residue on the panel ≤0.2mm, allowed	Film gauge	MIN
FPC defect	FPC wiring FPC golden finger		FPC, TCP damage / gold finger peroxidation, adhesive residue, not allowed	Visual	MIJ
			The height of burr edge of TCP punching surface ≧ 0.4mm, not allowed	Caliper	MIN
	FPC damage/crease		Damage and breaking, not allowed Crease does not affect the electrical performance display, allowed	Check by eyes	MIN

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Inspection item		Figure	Inspection standard	Inspection method	MAJ/ MIN
Protective film defect	Protective film	Scratch and crease on the surface but no affect to protection function, allowed		Check by eyes	MIN
		Adhesive at edge L≤5mm，W≤0.5mm，N=2, no entering into viewing area		Check by eyes	MIN
Stain defect	Stain	If stain can be normally wiped clean by > 99% alcohol, allowed		Visual	MIN
Pull tab defect	Pull tab	The position and direction meet the document requirements, and ensure that the protective film can be pulled off.		Check by eyes/ Manual pulling	MIN
Shading tape defect	Shading tape	Tilt≤10°, flat without warping, completely covering the IC.		Check by eyes/ Film gauge	MIN
Stiffener	Stiffener	Flat without warping, Exceeding the left and right edges of the FPC is not allowed. Left and right can be less than 0.5mm from FPC edge		Check by eyes	MIN
Label	Label/ Spraying code	The content meets the requirements of the work sheet. The attaching position meets the requirements of the technical documents.		Check by eyes	MIN

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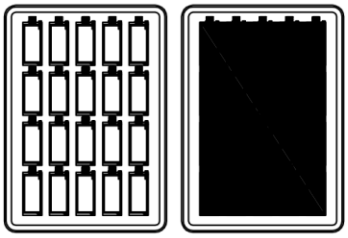
14. Packaging

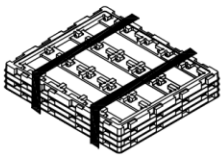
CUSTOMER'S APPROVED:	DATE:2023.02.06	PAGE: 1/1

PACKLING ORDER:

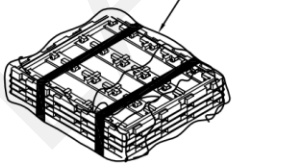
1) Putting 15 pcs Modules on each PET tray.Product with EPE pad on top.



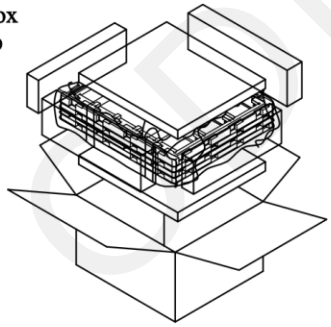
2) Putting 18 pcs PET trays together with 1 empty tray on the top of PET tray. the tray together with rubber band.



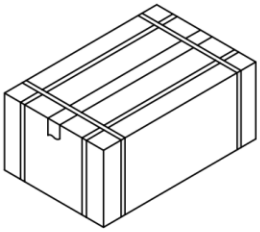
3) Insert in the ESD bag, add desiccant in the ESD bag. Plastic sealing.



4) Inside the outer box, The box is filled with EPE pad from top to bottom, front to back.



5) Packing finished



Note: 15 x (19−1) = 270 pcs/Outcarton

Dimension (Out carton): 500*350*205mm

	Drw:		Chk:		Apv:	

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15. Precautions

(1) Do not apply pressure to the EPD panel in order to prevent damaging it.

(2) Do not connect or disconnect the interface connector while the EPD panel is in operation.

(3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.

(4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.

(5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as "Ghosting" or "Image Sticking" may occur. It is recommended to refreshed the ESL /EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue

(6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.

(7) For more precautions, please click on the link:
https://www.good-display.com/news/80.html

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